

5. A microcomputer according to claim 2, wherein said non-volatile storage means is a single EEP-ROM.

6. A microcomputer according to claim 2, wherein said non-volatile storage means is a single EP-ROM.

7. A microcomputer according to claim 5, wherein said non-volatile storage means includes gate means for disabling transfer of at least one of an address and data from said central processing unit to said non-volatile storage means during a write period of said data transfer.

8. A microcomputer according to claim 1, wherein all constituent elements are implemented in a large-scale-integration semiconductor device.

9. A microcomputer comprising:
a central processing unit having memory address space;
an electrically programmable ROM into which both program and data can be written under direction of said central processing unit;
a memory for storing a write control program for controlling a write operation to said electrically programmable ROM;
a write control means for controlling the write operation to said electrically programmable ROM;
said electrically programmable ROM and said memory being disposed at mutually different address positions on the address space of said central processing unit.

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10. A microcomputer according to claim 9, wherein said write control means includes a latch means for retaining control signals to said electrically programmable ROM during a write period.

11. A microcomputer according to claim 9, wherein all constituent elements are implemented in a large-scale-integrated semiconductor device.

12. In a microcomputer comprising a central processing unit, an electrically programmable ROM in which both program and data can be written and a memory for storing a write control program, a method of writing data to said electrically programmable ROM, said method comprising the steps of:

(1) causing said central processing unit to jump from a program in said electrically programmable EP-ROM to a leading address of a write control program in said memory;

(2) executing a write control process in said electrically programmable ROM under the write control program;

(3) judging completion of the write operation in said central processing unit;

(4) returning said central processing unit from said memory to a program in said electrically programmable ROM.

13. The method of writing data according to claim 12, further comprising a step of controlling the judging by a flag generated from at least one of a write control unit and an interrupt request.

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14. A semiconductor integrated circuit device comprising:

a non-volatile storage means into which both program and data can be written;

a memory for storing a write control program for controlling a write operation to said non-volatile storage means;

control means having address space for controlling said non-volatile storage means and said memory; and

said non-volatile storage means and said memory being disposed at mutually different address positions on the address space of said control means.

15. A semiconductor integrated circuit device according to claim 14, wherein said memory for storing said write control program is ROM.

16. A semiconductor integrated circuit device according to claim 14, wherein said memory for storing said write control program is mask RAM.

17. A semiconductor integrated circuit device according to claim 14, wherein said control means is a central processing unit.

18. A semiconductor integrated circuit device according to claim 14, wherein said non-volatile storage means includes gate means for disabling transfer of at least one of an address and data input from said control means to said non-volatile storage means during the write operation.

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19. A semiconductor integrated circuit device according to claim 14, wherein said non-volatile storage means is a single EEP-ROM.

20. A semiconductor integrated circuit device according to claim 14, wherein said non-volatile storage means is a single EP-ROM.

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